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09/252,690	02/22/1999	KAZUYA YONEMOTO	P98-2697	4790

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EXAMINER	
HANNETT, JAMES M	

ART UNIT	PAPER NUMBER
2612	

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17

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/252,690	Applicant(s) YONEMOTO ET AL.	
	Examiner James M Hannett	Art Unit 2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 May 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 5/23/2003 have been fully considered but they are not persuasive. The applicants argument that the prior art does not teach the new limitation added to the claim that the solid state image pickup device has a plurality of signal lines, each of the signal lines being associated with corresponding pixels and each of said signal lines is used for both said reading operation and the shutter operation. It is viewed by the examiner that the plurality of signal lines are signal lines (133-horizontal gate line) and (135-vertical gate line) for pixel (1,1) Todaka et al teaches on Column 4, Lines 23-68. Todaka discusses that voltage signals are applied to both signal lines (133 and 135) for both the shutter operation and the pixel reading operation. Therefore, this constitutes each of the signal lines being associated with corresponding pixels and each of said signal lines is used for both said reading operation and the shutter operation. Furthermore, Todaka teaches the use of a single signal output line used for transmitting both image output signals and an output from the shutter operation for a pixel. As depicted in Figure 3, the output for a single pixel (113) is output through transistor (132) the output of transistor (132) is connected to signal lines (149) and (139) through a common signal line that is depicted in Figure 3 but has no reference character. The examiner views this signal line as the signal line that connects the output of transistor (132) to the input of transistors (137 and 138). This signal line is used for both a signal readout operation and a shutter operation.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1: Claims 1-5, 8-12, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by USPN 4,835,617 Todaka et al.

2: As for Claim 1, Todaka teaches on Column 1 the use of a MOS sensor-type image pickup device. Todaka teaches the use of an array of photodiodes arranged in a matrix form. Therefore, Todaka teaches the use of pixels having photoelectric conversion units to produce a signal from incident light arranged in rows and columns. Todaka teaches on Column 1, Lines 65-68 the use of a horizontal scanning circuit and a vertical scanning circuit. Todaka teaches on Columns 3 and 4, Lines 59-68 and Lines 1-5 that a reading operation for a signal of a pixel in one row and an electronic shutter operation or (resetting) for a signal in other row are carried out at the same time during one pixel period. It is viewed by the examiner that the plurality of signal lines are signal lines (133-horizontal gate line) and (135-vertical gate line) for pixel (1,1) Todaka et al teaches on Column 4, Lines 23-68. Todaka discusses that voltage signals are applied to both signal lines (133 and 135) for both the shutter operation and the pixel reading operation. Therefore, this constitutes each of the signal lines being associated with corresponding pixels and each of said signal lines is used for both said reading operation and the shutter operation. Todaka teaches the use of a single signal output line used for transmitting both image output signals and an output from the shutter operation for a pixel. As depicted in Figure 3, the output for a single pixel (113) is output through transistor (132) the output of transistor (132) is connected to signal lines (149) and (139) through a common signal line that is depicted in Figure 3 but has no reference character. The examiner views this signal line as the signal line that

connects the output of transistor (132) to the input of transistors (137 and 138). This signal line is used for both a signal readout operation and a shutter operation.

3: As for Claim 2, Todaka teaches on Column 4, Lines 1-5 that at the time the read scanning circuit reads the picture element (1, m), the reset scanning circuit resets or performs an electronic shutter operation on the picture element (1+n, m). Therefore, the reading operation of a signal of a pixel in one column in the one row (1, m) and an electronic shutter operation for a signal of a pixel in the one column in the other row (1+n, m) are performed at the same time.

4: In regards to Claim 3, Todaka teaches on Column 4, Lines 1-5 that at the time the read scanning circuit reads the picture element (1, m), the reset scanning circuit resets or performs an electronic shutter operation on the picture element (1+n, m). Todaka teaches on Column 4, Lines 23-43 that when the pixel at location (1, 2) is read an electronic shutter operation is performed for the pixel at location (2, 2). Next a read operation is performed for the pixel at location (1, 3) when an electronic shutter operation is performed for the pixel at location (2, 3). Therefore, the reading operation of a signal of a pixel in one column in the one row (1, 3) and an electronic shutter operation for a signal of a pixel in a column adjacent to the one column in the other row (2, 2) are performed at the same time.

5: In regards to Claim 4, Todaka teaches and depicts in Figure 3 that read scanning pulses and electronic shutter scanning pulses are supplied from both the horizontal and vertical scanning circuits. Todaka teaches that to read the data from the photodiode (113) or to perform an electronic shutter operation, pulses need to be supplied to the gates of MOS's (131), and (132) from the vertical scanning circuit and the horizontal scanning circuit.

6: As for Claim 5, Todaka teaches on Column 5, Lines 13-51 and depicts in Figure 5 that one pulse is supplied for each pixel as the read scanning pulse, and one pulse is supplied for each pixel as the electronic shutter scanning pulse. Todaka depicts in Figure 5 that the read scanning pulse and electronic shutter scanning pulse are supplied at a timing at which the phases of the read scanning pulse and the electronic shutter scanning pulse do not overlap.

7: As for Claim 8, Claim 8 is rejected for the reasons discussed above related to claim 1, since claim 8 is substantively equivalent to claim 1.

8: As for Claim 9, Claim 9 is rejected for the reasons discussed above related to claim 2, since claim 9 is substantively equivalent to claim 2.

9: In regards to Claim 10, Claim 10 is rejected for the reasons discussed above related to claim 3, since claim 10 is substantively equivalent to claim 3.

10: In regards to Claim 11, Claim 11 is rejected for the reasons discussed above related to claim 4, since claim 11 is substantively equivalent to claim 4.

11: As for Claim 12, Claim 12 is rejected for the reasons discussed above related to claim 5, since claim 12 is substantively equivalent to claim 5.

12: In regards to Claim 15, Todaka teaches on Column 2, Lines 65 the use of a camera comprising an image sensor, a lens, a stop, a driving circuit for driving the sensor, a camera circuit for producing a television signal from the output of the image sensor and a control circuit. Todaka teaches on Column 1 the use of a MOS sensor-type image pickup device. Todaka teaches the use of an array of photodiodes arranged in a matrix form. Therefore, Todaka teaches the use of pixels having photoelectric conversion units to produce a signal from incident light arranged in rows and columns. Todaka teaches on Column 1, Lines 65-68 the use of a horizontal scanning

circuit and a vertical scanning circuit. Todaka teaches on Columns 3 and 4, Lines 59-68 and Lines 1-5 that a reading operation for a signal of a pixel in one row and an electronic shutter operation or (resetting) for a signal in other row are carried out at the same time during one pixel period. It is viewed by the examiner that the plurality of signal lines are signal lines (133-horizontal gate line) and (135-vertical gate line) for pixel (1,1) Todaka et al teaches on Column 4, Lines 23-68. Todaka discusses that voltage signals are applied to both signal lines (133 and 135) for both the shutter operation and the pixel reading operation. Therefore, this constitutes each of the signal lines being associated with corresponding pixels and each of said signal lines is used for both said reading operation and the shutter operation. Todaka teaches the use of a single signal output line used for transmitting both image output signals and an output from the shutter operation for a pixel. As depicted in Figure 3, the output for a single pixel (113) is output through transistor (132) the output of transistor (132) is connected to signal lines (149) and (139) through a common signal line that is depicted in Figure 3 but has no reference character. The examiner views this signal line as the signal line that connects the output of transistor (132) to the input of transistors (137 and 138). This signal line is used for both a signal readout operation and a shutter operation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13: Claims 6, 7, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 4,835,617 Todaka et al in view of USPN 4,954,895 Akimoto et al.

14: As for Claim 6, Todaka teaches and depicts in Figure 3 that to read the data from the photodiode (113) pulses need to be supplied to the gates of MOS's (131), and (132) from the vertical scanning circuit and the horizontal scanning circuit. Todaka teaches an operation of reading a signal charge obtained by the pixel in the photoelectric conversion unit (113), to a signal line (149) is controlled by the product between a vertical scanning pulse (OY1) and a horizontal read pulse (OX1). Todaka teaches and depicts in Figure 3 that read scanning pulses and electronic shutter scanning pulses are supplied from both the horizontal and vertical scanning circuits. Todaka teaches that to read the data from the photodiode (113) or to perform an electronic shutter operation, pulses need to be supplied to the gates of MOS's (131), and (132) from the vertical scanning circuit and the horizontal scanning circuit.

Todaka is silent on the use of connecting to the signal line a charge detection amplifier for converting the read signal charge into a voltage signal.

Akimoto et al teaches on Column 11, Lines 30-34 that it is commonly known in the art to have an amplifier on the signal line to enable the charge from the photoelectric conversion element to be amplified and converted into a voltage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a charge detection amplifier as taught by Akimoto et al connected to the signal line of Todaka et al in order to enable the charge from the photoelectric conversion element to be amplified and converted into a voltage.

15: In regards to Claim 7, Todaka teaches on Column 5, Lines 13-51 and depicts in Figure 5 that one pulse is supplied for each pixel as the read scanning pulse, and one pulse is supplied for each pixel as the electronic shutter scanning pulse. Todaka depicts in Figure 5 that the read scanning pulse and electronic shutter scanning pulse are supplied at a timing at which the phases of the read scanning pulse and the electronic shutter scanning pulse do not overlap.

16: As for Claim 13, Claim 13 is rejected for the reasons discussed above related to claim 6, since claim 13 is substantively equivalent to claim 6.

17: In regards to Claim 14, Claim 14 is rejected for the reasons discussed above related to claim 7, since claim 7 is substantively equivalent to claim 14.

Conclusion

This is a request for continued examination of applicant's earlier Application No. 09/252,690. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however,

event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M Hannett whose telephone number is 703-305-7880. The examiner can normally be reached on 8:00 am to 5:00 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on 703-305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James M. Hannett
Examiner
Art Unit 2612

JMH
May 5, 2004

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